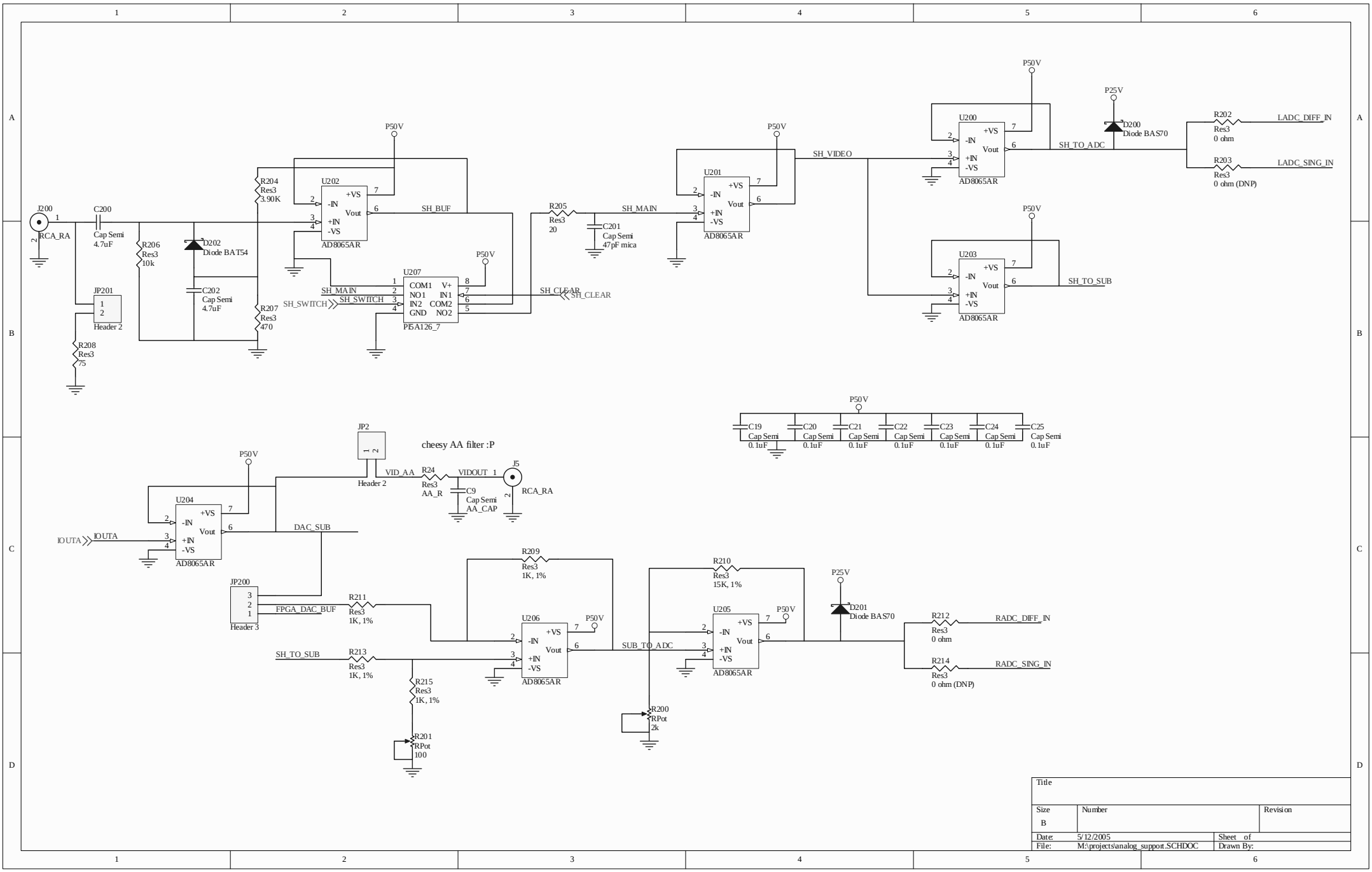
J200
RCA_RA
C200
Cap Semi
4.7uF
R206
Res3
10k
D202
Diode BAT54
C202
Cap Semi
4.7uF
JP201
Header 2
R208
Res3
75
R207
Res3
470
R204
Res3
3.90K
U202
AD8065AR
P50V
SH_BUF
SH_MAIN
SH_SWITCH
U207
PI5A126_7
SH_CLEAR
R205
Res3
20
C201
Cap Semi
47pF mica
U201
AD8065AR
SH_VIDEO
U200
AD8065AR
SH_TO_ADC
P25V
D200
Diode BAS70
R202
Res3
0 ohm
LADC_DIFF_IN
R203
Res3
0 ohm (DNP)
LADC_SING_IN
U203
AD8065AR
SH_TO_SUB
C19
C20
C21
C22
C23
C24
C25
Cap Semi
0.1uF
JP2
Header 2
cheesy AA filter :P
VID_AA
R24
Res3
AA_R
C9
Cap Semi
AA_CAP
VIDOUT
J5
RCA_RA
U204
AD8065AR
IOUTA
DAC_SUB
JP200
Header 3
FPGA_DAC_BUF
R211
Res3
1K, 1%
R209
Res3
1K, 1%
R210
Res3
15K, 1%
U206
AD8065AR
U205
AD8065AR
SUB_TO_ADC
R213
Res3
1K, 1%
R215
Res3
1K, 1%
R201
RPot
100
R200
RPot
2k
D201
Diode BAS70
R212
Res3
0 ohm
RADC_DIFF_IN
R214
Res3
0 ohm (DNP)
RADC_SING_IN
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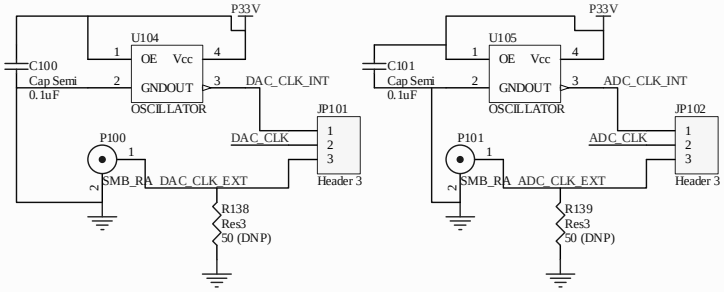
Size
B
Number
Revision
Date:
5/12/2005
Sheet of
File:
M:\projects\analog_support.SCHDOC
Drawn By:



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Size: B	Number	Revision
Date: 5/12/2005		Sheet of
File: M:\projects\clocks.SCHDOC		Drawn By:

track and hold
unity gain buffers
DAC expt with res, with current mirror
8-bit DAC
hyst. reset switch
voltage subtractor

dummy H8 area for experiments

bits0-3,1 trim, 4x16
6-bit DAC

U103A
XC3S400-5PQ208C

BANK 0
BANK 1
BANK 2
BANK 3
BANK 4
BANK 5
BANK 6
BANK 7

P33V
R100
Res2
15.4 1%
JP100
Header 3
FPGA_DAC_OUT
R101
Res2
15.4 1%
FPGA_DAC_RAW
Q100
HFA3046B

U100
P50V
FPGA_DAC_OUT
FPGA_DAC_BUF
AD8065AR

U101
P50V
R102
RPot
1K
RADC_VREF
AD8065AR

U102
P50V
R103
RPot
1K
LADC_VREF
AD8065AR

LADC_DIFF_IN
LADC_SING_IN
LADC_VREF
RADC_SING_IN
RADC_DIFF_IN
RADC_VREF

SA15
SA16
SCE_N
SWE_N
SOE_N
SA17
SA2
SA3
SA12

LADC_14
LADC_13
LADC_12
LADC_11
LADC_10
LADC_9
LADC_8
LADC_7
LADC_6
LADC_5
LADC_4
LADC_3
LADC_2
LADC_1
LADC_0

RADC_14
RADC_13
RADC_12
RADC_11
RADC_10
RADC_9
RADC_8
RADC_7
RADC_6
RADC_5
RADC_4
RADC_3
RADC_2
RADC_1
RADC_0

R104 100 ohm 1%
R105 100 ohm 1%
R106 100 ohm 1%
R107 100 ohm 1%
R109 100 ohm 1%
R112 100 ohm 1%
R114 100 ohm 1%
R117 100 ohm 1%
R119 100 ohm 1%
R121 100 ohm 1%
R123 100 ohm 1%
R125 100 ohm 1%
R127 100 ohm 1%
R130 100 ohm 1%
R132 100 ohm 1%
R134 100 ohm 1%

R108 100 ohm 1%
R110 100 ohm 1%
R111 100 ohm 1%
R113 100 ohm 1%
R115 100 ohm 1%
R116 100 ohm 1%
R120 100 ohm 1%
R122 100 ohm 1%
R124 100 ohm 1%
R126 100 ohm 1%
R128 100 ohm 1%
R129 100 ohm 1%
R131 100 ohm 1%
R133 100 ohm 1%
R135 100 ohm 1%

R23 50
R136 50
R137 50

DAC_CK
SRAM_CLK
ADC_CLK

SA4 SA5 SA18 SA6 SA1 SA0 SA9 SA7 SA8 SA14 SA10 SA11 SA13

SRAM_CLK
ADC_CLK
DAC_CK
PROG_INIT_N
SH_CLEAR
PROG_DIN

PCB Rule
PCB Rule

Impedance Constraint [Min = 70.00 Max = 80.00]
Routing Topology [Topology - Daisy-Simple]

Title		
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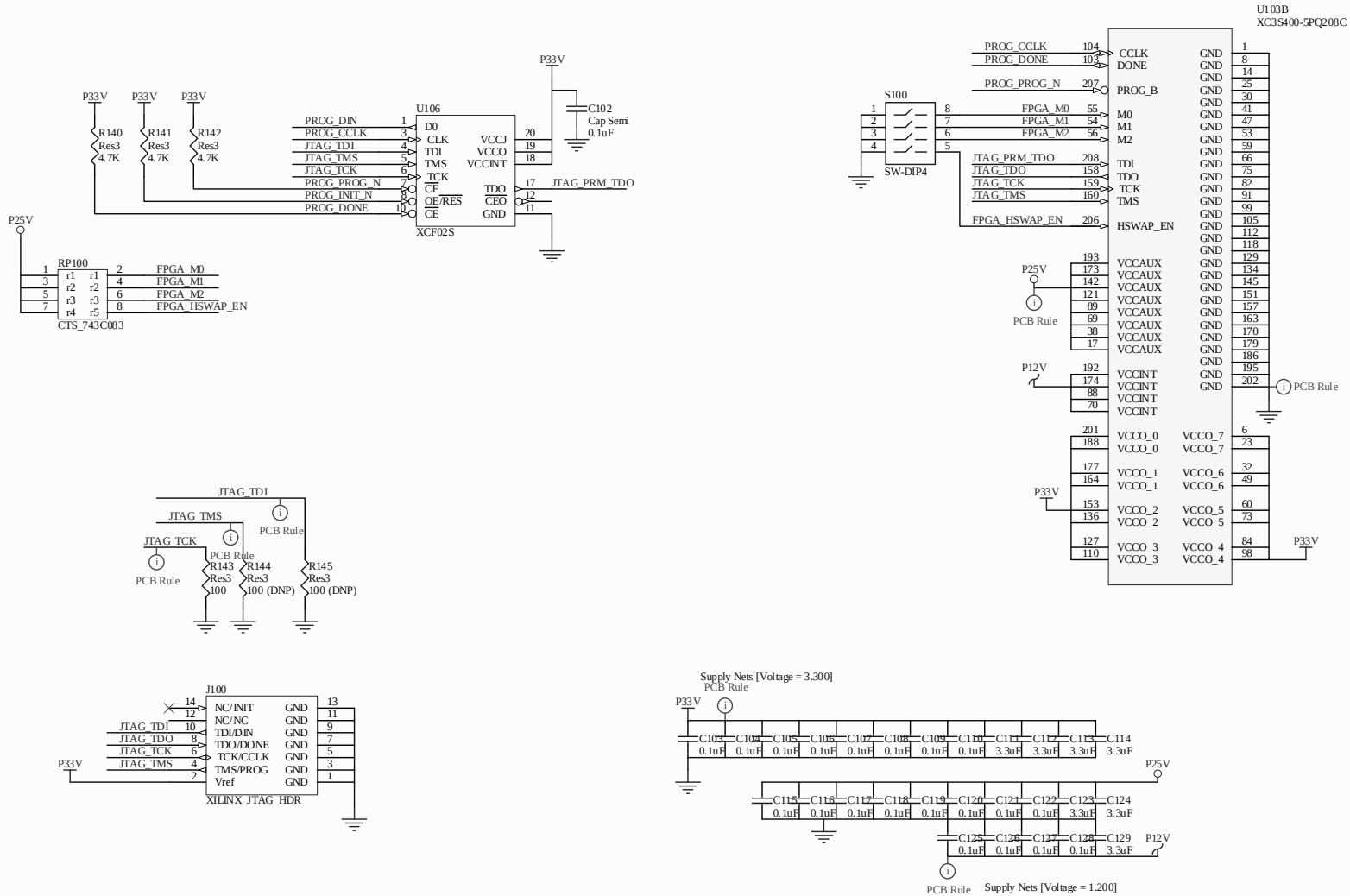

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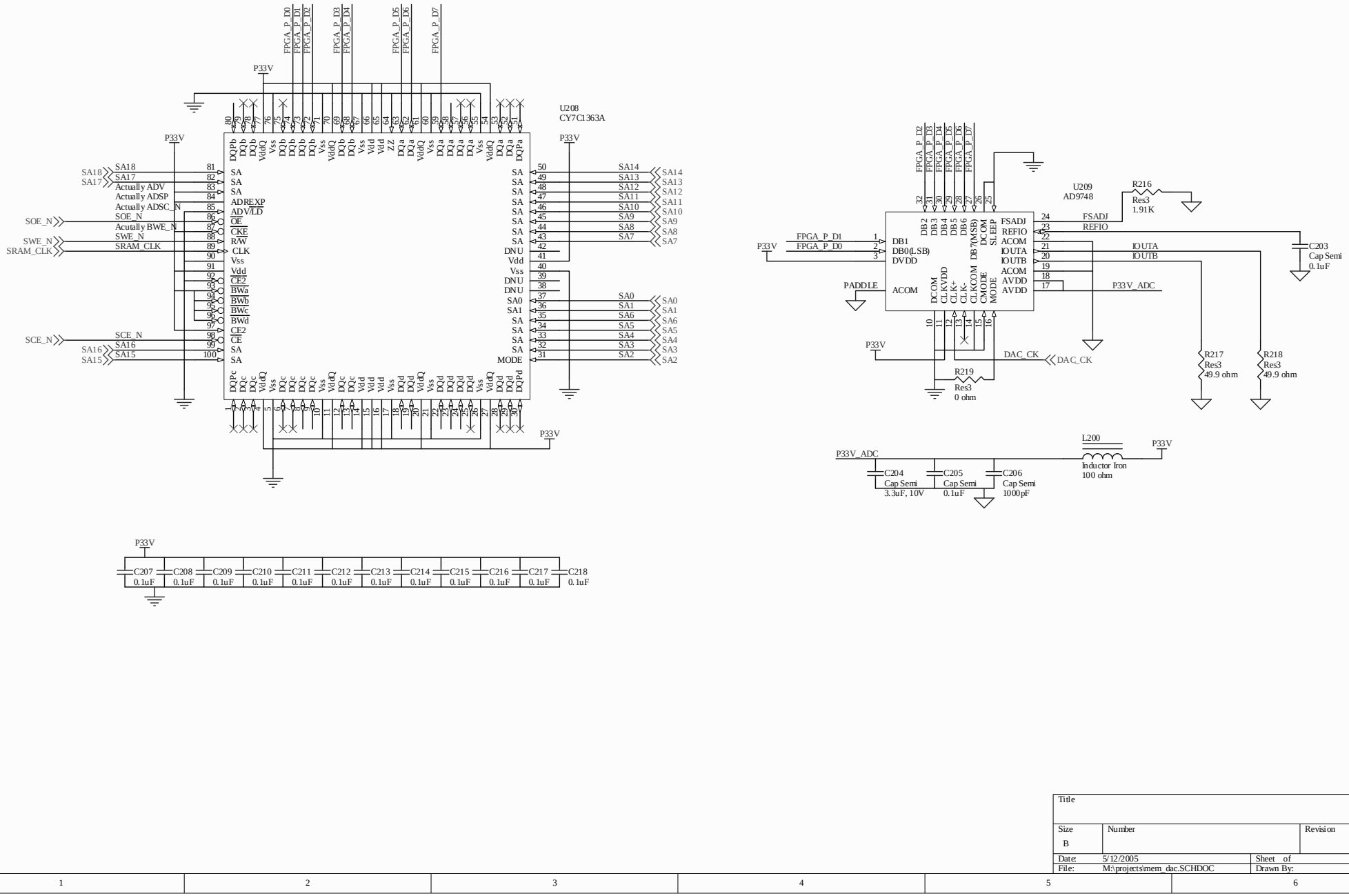

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Date: 5/12/2005		Sheet of
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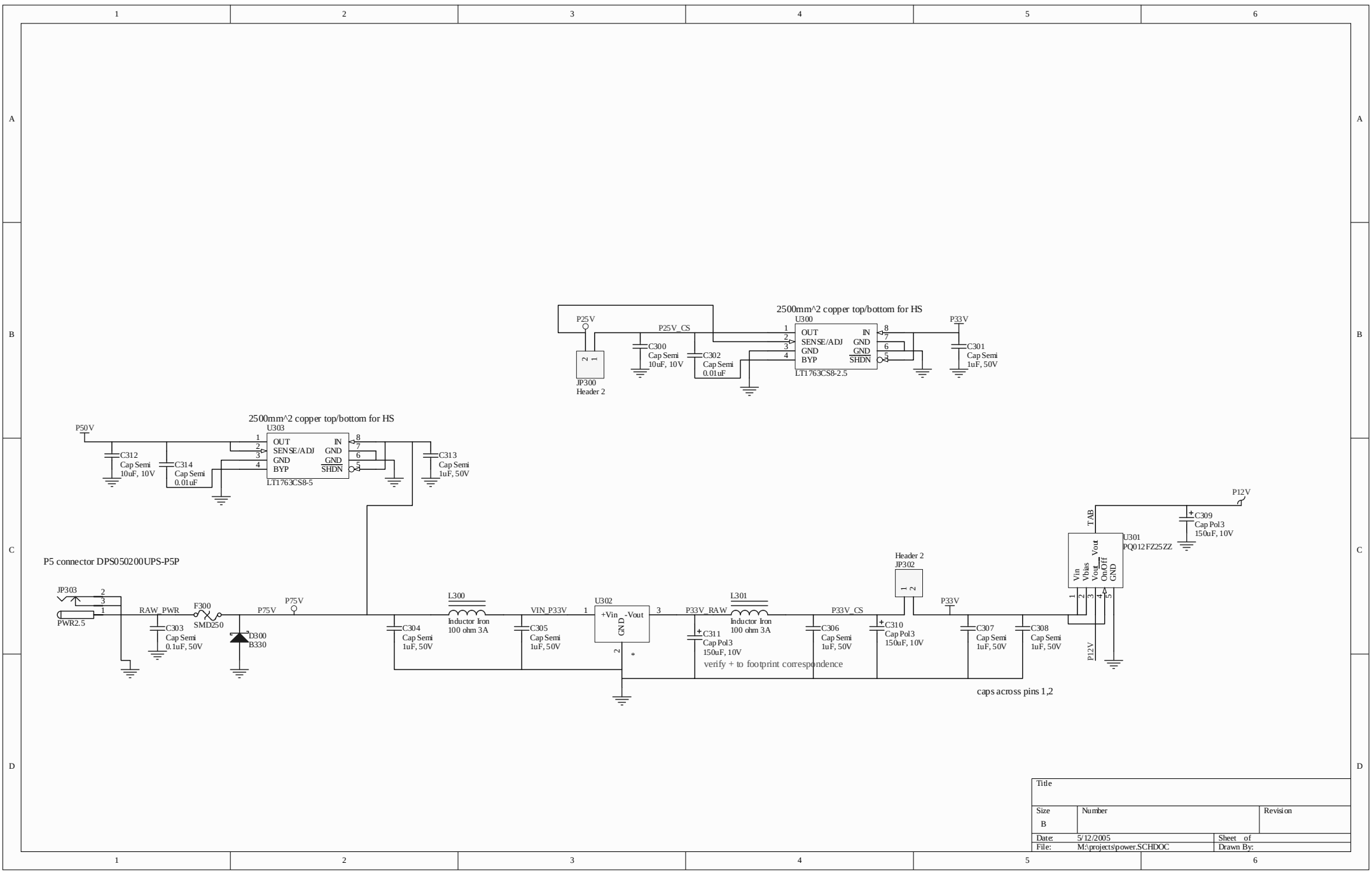
2500mm^2 copper top/bottom for HS
P25V
P25V_CS
U300
OUT
SENSE/ADJ
GND
BYP
IN
GND
GND
SHDN
LT1763CS8-2.5
P33V
C300
Cap Semi
10uF, 10V
C302
Cap Semi
0.01uF
C301
Cap Semi
1uF, 50V
JP300
Header 2
2500mm^2 copper top/bottom for HS
P50V
U303
OUT
SENSE/ADJ
GND
BYP
IN
GND
GND
SHDN
LT1763CS8-5
C312
Cap Semi
10uF, 10V
C314
Cap Semi
0.01uF
C313
Cap Semi
1uF, 50V
P5 connector DPS050200UPS-P5P
JP303
PWR2.5
RAW_PWR
F300
SMD250
P75V
C303
Cap Semi
0.1uF, 50V
D300
B330
L300
Inductor Iron
100 ohm 3A
C304
Cap Semi
1uF, 50V
VIN_P33V
U302
+Vin
-Vout
GND
C305
Cap Semi
1uF, 50V
P33V_RAW
L301
Inductor Iron
100 ohm 3A
C311
Cap Pol3
150uF, 10V
verify + to footprint correspondence
P33V_CS
C306
Cap Semi
1uF, 50V
Header 2
JP302
C310
Cap Pol3
150uF, 10V
P33V
C307
Cap Semi
1uF, 50V
C308
Cap Semi
1uF, 50V
caps across pins 1,2
P12V
TAB
U301
PQ012FZ25ZZ
Vin
Vbias
Vout
On/Off
GND
C309
Cap Pol3
150uF, 10V
Title
Size
B
Number
Revision
Date: 5/12/2005
Sheet of
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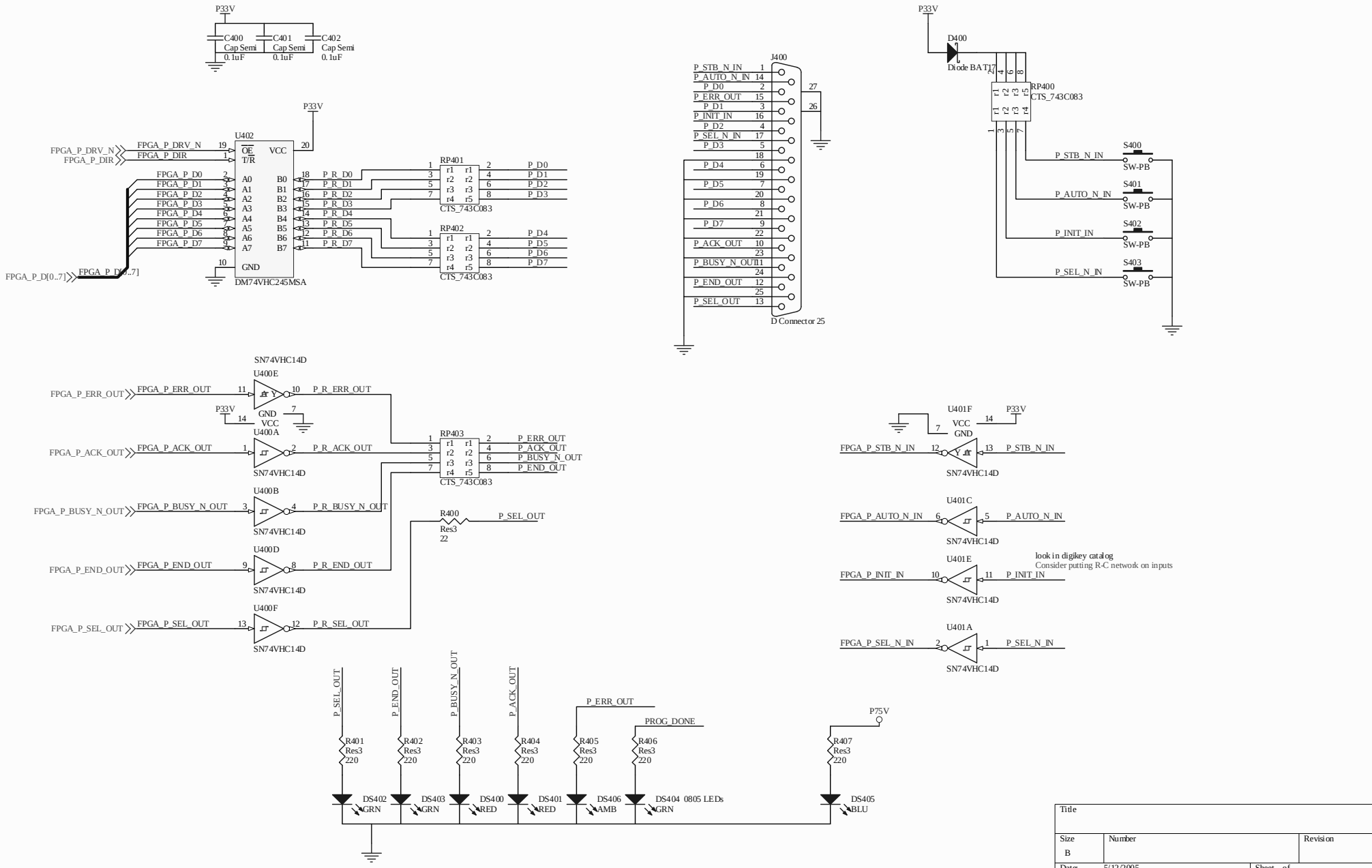
Drawn By:


P33V
C400 Cap Semi 0.1uF
C401 Cap Semi 0.1uF
C402 Cap Semi 0.1uF
U402
DM74VHC245MSA
RP401
RP402
CTS_743C083
J400
D Connector 25
D400
Diode BAT17
RP400
CTS_743C083
S400
S401
S402
S403
SW-PB
U400E
U400A
U400B
U400D
U400F
SN74VHC14D
RP403
R400
Res3
22
U401F
U401C
U401E
U401A
look in digikey catalog
Consider putting R-C network on inputs
P75V
R401 Res3 220
R402 Res3 220
R403 Res3 220
R404 Res3 220
R405 Res3 220
R406 Res3 220
R407 Res3 220
DS402 GRN
DS403 GRN
DS400 RED
DS401 RED
DS406 AMB
DS404 0805 LEDs GRN
DS405 BLU
Title
Size B
Number
Revision
Date: 5/12/2005
Sheet of
File: M:\projects\pport.SCHDOC
Drawn By:

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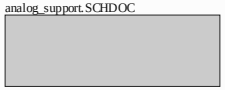
analog_support.SCHDOC



U_clocks
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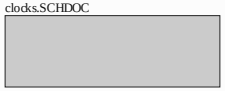

U_fpga_main
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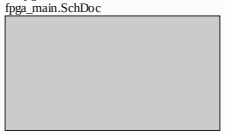

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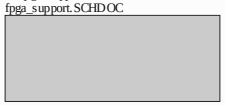
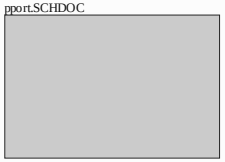


U_pport
pport.SCHDOC



U_mem_dac
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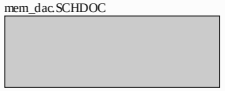
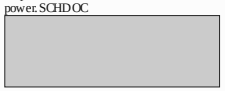


U_power
power.SCHDOC



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