

Advanced Embedded Microcontroller Seminar--Day 2

Andrew Huang
bunnie@mit.edu

1/21/99

Microcontroller Seminar -- ASH

1

Agenda

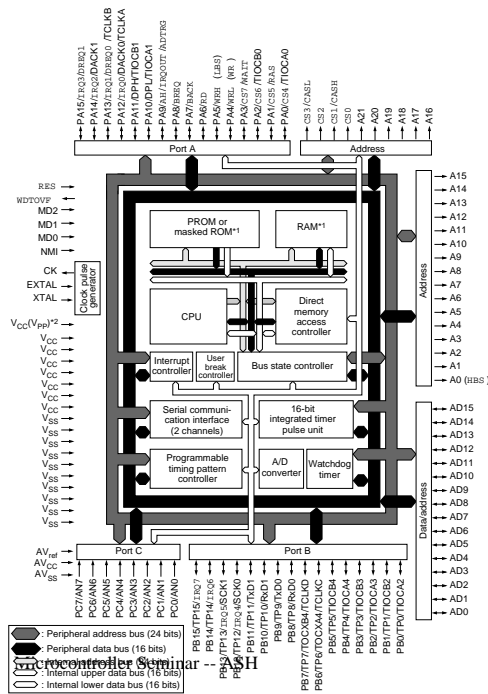
- Day 2: 1/21
 - Designing the SH-1 into your system
 - Details of the SH1 integrated peripherals
 - Overview of the SH1WH, on-board peripheral specs
 - development environment

1/21/99

Microcontroller Seminar -- ASH

2

SH-1 Block Diagram



1/21/99

3

Location of Hardware Manual

- http://semiconductor.hitachi.com/products/h_micon/1_sh/1_sh1/H11TH003D3/pdf/h1103.pdf
 - difficult to read sometimes, but the comprehensive source of information on the SH-1
 - today's lecture distills and presents some of the most important concepts to get you started

1/21/99

Microcontroller Seminar -- ASH

4

Getting in to the SH-1: Features

- 32-bit RISC CPU with MAC instruction
- interrupt controller
 - 9 external interrupt pins
 - 31 internal interrupt sources
 - 16 priority levels
- user break controller
 - for trapping on special conditions, debugging
- clock generator
 - drives an external crystal to make internal timebase
- bus state controller
 - 8/16 bit accesses
 - muxed or separate address and data
 - controls DRAM, SRAM, ROM, or peripherals
 - generates up to 8 chip selects
 - wait states
- DMA controller
 - 4 channels, 2 internal, 2 external
 - transfer between external and internal memory, I/O
 - cycle-steal and burst-mode

1/21/99

Microcontroller Seminar -- ASH

5

- 16-bit integrated timer unit
 - measures input pulse widths
 - generates PWM, complementary PWM
 - phase counting mode
- timing pattern controller
 - can be used in conjunction with DMAC and ITU to generate arbitrary pulse trains with no load on CPU
 - non-overlapping mode available
 - applications include multi-phase motor control, serial communications (SPI, microwire, etc.)
- watchdog timer
- serial comm. interface
 - 2 channels
 - async/synch options
 - internal baud rate generator
- A/D converter
 - 10 bits, 8 channels
 - external trigger, reference source
- digital I/O ports
 - up to 40 lines, but all shared with other I/O functions
- on-chip RAM/ROM
 - SH7032 (ROM-less) has 8K RAM
 - SH7034 has 64K PROM plus 4K RAM
 - single-cycle access to on-chip RAM/ROM

1/21/99

Microcontroller Seminar -- ASH

6

SH-1: Key Design Point

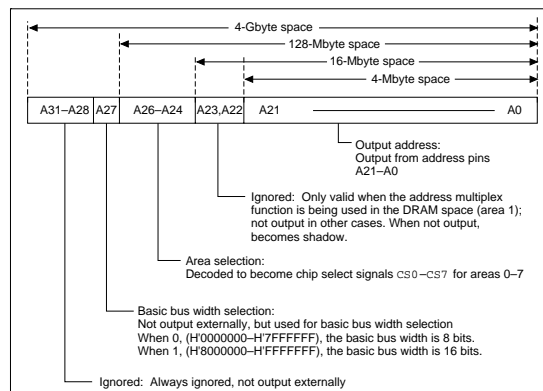
- All peripherals and memory are mapped to one common address space
 - 28-bit effective address space is divided into 16 equally sized sectors
 - 28 bits because top 4 bits of a 32-bit address are don't care
 - actual usage of allocated space per sector varies; undesignated areas alias to designated areas
 - processor bus behavior (ie, 8 or 16 bit mode, wait states, multiplexed adr, data) determined by which address is accessed
 - details of behavior can be modified by setting memory-mapped registers in the BSC
- Vector table is located at bottom of memory
 - hence there must always be a ROM mapped to CS0

1/21/99

Microcontroller Seminar -- ASH

7

Memory organization of the SH-1



1/21/99

Microcontroller Seminar -- ASH

8

Function allocation in the SH-1

Area	Address	Assignable Memory	Capacity (Linear Space)	Bus Width	CS Output
0	H'000000-H'0FFFFFFF	On-chip ROM ¹	64 kB	32	—
		External memory ²	4 MB	8/16 ³	CS0
1	H'1000000-H'1FFFFFFF	External memory	4 MB	8	CS1
		DRAM ⁴	16 MB	8	RAS CAS
2	H'2000000-H'2FFFFFFF	External memory	4 MB	8	CS2
3	H'3000000-H'3FFFFFFF	External memory	4 MB	8	CS3
4	H'4000000-H'4FFFFFFF	External memory	4 MB	8	CS4
5	H'5000000-H'5FFFFFFF	On-chip supporting modules	512 B	8/16 ⁵	—
6	H'6000000-H'6FFFFFFF	External memory ⁷	4 MB	8/16 ⁶	CS6
		Multiplexed I/O	4 MB		
7	H'7000000-H'7FFFFFFF	External memory	4 MB	8	CS7
0	H'8000000-H'8FFFFFFF	On-chip ROM ¹	64 kB	32	—
		External memory ²	4 MB	8/16 ³	CS0
1	H'9000000-H'9FFFFFFF	External memory	4 MB	16	CS1
		DRAM ⁴	16 MB	16	RAS CAS
2	H'A000000-H'AFFFFFFFFF	External memory	4 MB	16	CS2
3	H'B000000-H'BFFFFFFFF	External memory	4 MB	16	CS3
4	H'C000000-H'CFFFFFFFF	External memory	4 MB	16	CS4
5	H'D000000-H'DFFFFFFF	External memory	4 MB	16	CS5
6	H'E000000-H'EFFFFFFFFF	External memory	4 MB	16	CS6
7	H'F000000-H'FFFFFFF	On-chip RAM	8 kB ⁸ , 4 kB ⁹	32	—

1/21/99

Microcontroller Seminar -- ASH

9

BSC registers

Name	Abbr.	R/W	Initial Value	Address*1	Bus width
Bus control register	BCR	R/W	H'0000	H'5FFFA0	8,16,32
Wait state control register 1	WCR1	R/W	H'FFFF	H'5FFFA2	8,16,32
Wait state control register 2	WCR2	R/W	H'FFFF	H'5FFFA4	8,16,32
Wait state control register 3	WCR3	R/W	H'F800	H'5FFFA6	8,16,32
DRAM area control register	DCR	R/W	H'0000	H'5FFFA8	8,16,32
Parity control register	PCR	R/W	H'0000	H'5FFFAA	8,16,32
Refresh control register	RCR	R/W	H'0000	H'5FFFA C	8,16,32*2
Refresh timer control/status register	RTCSR	R/W	H'0000	H'5FFFA E	8,16,32*2
Refresh timer counter	RTCNT	R/W	H'0000	H'5FFFB0	8,16,32*2
Refresh time constant register	RTCOR	R/W	H'00FF	H'5FFFB2	8,16,32*2

1/21/99

Microcontroller Seminar -- ASH

10

Registers of the BSC

- BCR
 - determines basic signal configuration (DRAM mode on area 1, mux'd adr/data on area 6, warp mode, RD# duty cycle, byte access style)
- WCR[1:3]
 - configures wait states for normal, DMA accesses
- DCR
 - configures basic DRAM access timing (dual CAS, precharge time, FPM, CAS duty cycle)
- RCR
 - configures DRAM refresh timing (CBR, self-refresh, wait states)
- RTCSR, RTCNT
 - configures refresh period based on system clock
- PCR
 - configures parity checking modes

1/21/99

Microcontroller Seminar -- ASH

11

PFC

- Pin function controller
 - determines functions of multiplexed pins
 - almost every I/O pin has multiple functions
 - must initialize to select proper mode prior to using any peripheral function
 - many basic services, such as some chip select lines, RD#, WR#, CAS/RAS can be turned on or off by writing to this register
 - fastest way to wedge the system is to write the wrong info to these registers

1/21/99

Microcontroller Seminar -- ASH

12

PFC registers

Name	Abbreviation	R/W	Initial Value	Address	Access Size
Port A I/O register	PAIOR	R/W	H'0000	H5FFFFC4	8, 16, 32
Port A control register 1	PACR1	R/W	H'3302	H5FFFFC8	8, 16, 32
Port A control register 2	PACR2	R/W	H'FF95	H5FFFFCA	8, 16, 32
Port B I/O register	PBIOR	R/W	H'0000	H5FFFFC6	8, 16, 32
Port B control register 1	PBCR1	R/W	H'0000	H5FFFFCC	8, 16, 32
Port B control register 2	PBCR2	R/W	H'0000	H5FFFFCE	8, 16, 32
Column address strobe pin control register	CASCR	R/W	H5FFF	H5FFFFEE	8, 16, 32

- P{A,B}CR{1,2} configures which mux'd function to use
- P{A,B}IOR configures, on a pin by pin basis, input or output mode if digital I/O mode is selected
- CASCR determines function of mux'd CS1,3 and CASL,H lines

Digital I/O

- Referred to as parallel I/O in the hardware manual
 - any of port A or B can be configured to be input or output
 - port C is input only
 - ports A and B are each 16 bits wide at max, port C is 8 bits wide at max
 - port C is mux'd with analog input, and automatically functions as analog input when A/D is activated
- PADR, PBDR, and PCDR are R/W registers that will either reflect the data on the pin, or contain the data to be driven on pin, depending on pin configuration

Interrupt Controller

- 16 priority levels
- up to 255 interrupt vectors
 - about 43 are actually assigned to interrupt sources
 - vector table starts at memory location 0, each vector consisting of a 32-bit pointer to code to handle the interrupt
 - power on reset and manual reset each has two vectors, the first for setting the PC, the second for setting the SP
- 8 external interrupt inputs
- IRQOUT line to indicate presence of internal interrupts
- edge or level triggered, programmable by software

1/21/99

Microcontroller Seminar -- ASH

15

Interrupts

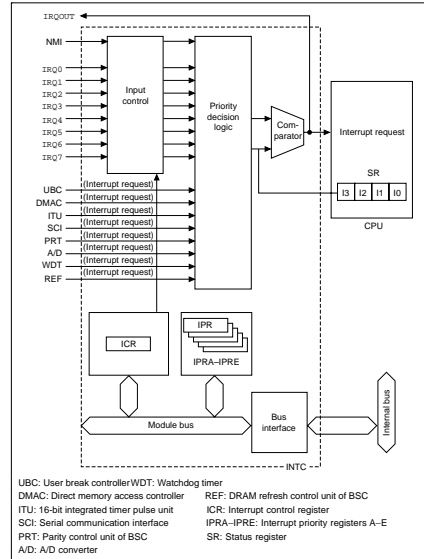
- on interrupt,
 - status register is pushed (32-bit)
 - return PC is pushed (32-bit)
 - note that SP should always be a multiple of 4
- interrupt response latency
 - latency dependant upon how fast long word accesses to memory occur
 - min. latency is 11 cycles (8 cycles for internal pipes to flush, plus 3 cycles for vector fetch and stack pushes)
 - max. latency is $12 + 2(\text{SR, PC, vector access times}) + \text{fetch time for first handler instruction}$
 - typ. latency around 1 to 2 us using slow memory at 12 MHz
- see table 4.10 in hardware manual for precise behavior of machine on a wide range of conditions

1/21/99

Microcontroller Seminar -- ASH

16

Interrupt Controller Hardware

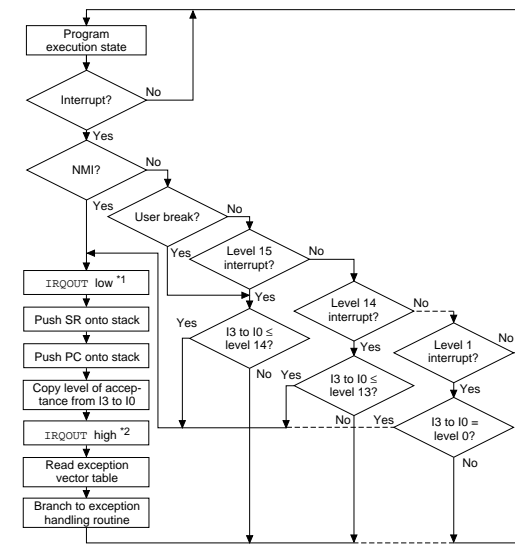


1/21/99

Microcontroller Seminar -- ASH

17

Interrupt Processing Flow Chart



I3 to I0 : Interrupt mask bits of status register

1/21/99

Microcontroller Seminar -- ASH

18

Interrupt Controller Registers

Name	Abbr.	R/W	Address* ²	Initial Value	Bus width
Interrupt priority register A	IPRA	R/W	H'5FFFF84	H'0000	8, 16, 32
Interrupt priority register B	IPRB	R/W	H'5FFFF86	H'0000	8, 16, 32
Interrupt priority register C	IPRC	R/W	H'5FFFF88	H'0000	8, 16, 32
Interrupt priority register D	IPRD	R/W	H'5FFFF8A	H'0000	8, 16, 32
Interrupt priority register E	IPRE	R/W	H'5FFFF8C	H'0000	8, 16, 32
Interrupt control register	ICR	R/W	H'5FFFF8E	* ¹	8, 16, 32

Notes: 1. H'8000 when pin NMI is high, H'0000 when pin NMI is low.

Register	Bits 15-12	Bits 11-8	Bits 7-4	Bits 3-0
IPRA	IRQ0	IRQ1	IRQ2	IRQ3
IPRB	IRQ4	IRQ5	IRQ6	IRQ7
IPRC	DMAC0, DMAC1	DMAC2, DMAC3	ITU0	ITU1
IPRD	ITU2	ITU3	ITU4	SCIO
IPRE	SCI1	PRT* ¹ , A/D	WDT, REF* ²	(Reserved)* ³

- ICR sets NMI detection parameters and edge or level trigger of external interrupt sources

Programming the Vector Table

- Vector table is located in FLASH ROM
 - requires erasing part of ROM monitor and reprogramming
 - utilities will be provided to assist in this risky process
 - once your handler is debugged, it is recommended to burn it into some unused sector of FLASH so as to avoid accidental corruption

Integrated Timer Pulse Unit

Item	Channel 0	Channel 1	Channel 2	Channel 3	Channel 4
Counter clocks	Internal: ϕ , $\phi/2$, $\phi/4$, $\phi/8$ External: Independently selectable from TCLKA, TCLKB, TCLKC, and TCLKD				
General registers (output compare/ input capture dual registers)	GRA0, GRB0	GRA1, GRB1	GRA2, GRB2	GRA3, GRB3	GRA4, GRB4
Buffer registers	No	No	No	BRA3, BRB3	BRA4, BRB4
Input/output pins	TIOCA0, TIOCB0	TIOCA1, TIOCB1	TIOCA2, TIOCB2	TIOCA3, TIOCB3	TIOCA4, TIOCB4
Output pins	No	No	No	No	TOCXA4, TOCXB4
Counter clear function (compare match or input capture)	GRA0/GRB0	GRA1/GRB1	GRA2/GRB2	GRA3/GRB3	GRA4/GRB4
0	Yes	Yes	Yes	Yes	Yes
1	Yes	Yes	Yes	Yes	Yes
Toggle output	Yes	Yes	No	Yes	Yes
Input capture function	Yes	Yes	Yes	Yes	Yes
Synchronization	Yes	Yes	Yes	Yes	Yes
PWM mode	Yes	Yes	Yes	Yes	Yes
Reset-synchronized PWM mode	No	No	No	Yes	Yes
Complementary PWM mode	No	No	No	Yes	Yes
Phase counting mode	No	No	Yes	No	No
Buffer operation	No	No	No	Yes	Yes
DMAC activation	GRA0 compare match or input capture	GRA1 compare match or input capture	GRA2 compare match or input capture	GRA3 compare match or input capture	No
Interrupt sources (three)	<ul style="list-style-type: none"> • Compare match/input capture A0 • Compare match/input capture B0 • Overflow 	<ul style="list-style-type: none"> • Compare match/input capture A1 • Compare match/input capture B1 • Overflow 	<ul style="list-style-type: none"> • Compare match/input capture A2 • Compare match/input capture B2 • Overflow 	<ul style="list-style-type: none"> • Compare match/input capture A3 • Compare match/input capture B3 • Overflow 	<ul style="list-style-type: none"> • Compare match/input capture A4 • Compare match/input capture B4 • Overflow

1/21/99

Microcontroller Seminar -- ASH

21

ITU Registers

ChannelName	Abbreviation	R/W	Initial Value	Address ^{*1}	Access Size	
Shared	Timer start register	TSTR	R/W	H'E0/H'60	H5FFFF00 8	
	Timer synchro register	TSNC	R/W	H'E0/H'60	H5FFFF01 8	
	Timer mode register	TMDR	R/W	H'80/H'00	H5FFFF02 8	
	Timer function control register	TFCR	R/W	H'C0/H'40	H5FFFF03 8	
	Timer output control register	TOCR	R/W	H'FF/H'7F	H5FFFF31 8	
3	Timer control register 3	TCR3	R/W	H'80/H'00	H5FFFF22 8	
	Timer I/O control register 3	TIOR3	R/W	H'88/H'08	H5FFFF23 8	
	Timer interrupt enable register 3	TIER3	R/W	H'F8/H'78	H5FFFF24 8	
	Timer status register 3	TSR3	R/(W) ²	H'F8/H'78	H5FFFF25 8	
	Timer counter 3	TCNT3	R/W	H'00	H5FFFF26	8, 16
					H5FFFF27	8, 16
	General register A3	GRA3	R/W	H'FF	H5FFFF28	8, 16, 32
					H5FFFF29	8, 16, 32
	General register B3	GRB3	R/W	H'FF	H5FFFF2A	8, 16, 32
					H5FFFF2B	8, 16, 32
	Buffer register A3	BRA3	R/W	H'FF	H5FFFF2C	8, 16, 32
					H5FFFF2D	8, 16, 32
	Buffer register B3	BRB3	R/W	H'FF	H5FFFF2E	8, 16, 32
					H5FFFF2F	8, 16, 32

1/21/99

Microcontroller Seminar -- ASH

22

ITU Register Cross-Reference Matrix

See tables at end of ITU section in hardware manual for complete matrix

Operating Mode	Register Setting											
	TSNC	TMDR	TFGR			TOCR		TIOR0		TCR0		
	Sync	MDF	FDIR	PWM	PWM	PWM	Buffer	Select	IOA	IOB	Clear Select	Clock Select
Synch-ronized preset	SYNCD = 1	—	—	√	—	—	—	—	√	√	√	√
PWM	√	—	—	PWM0 = 1	—	—	—	—	—	√	√	√
Output compare A function	√	—	—	PWM0 = 0	—	—	—	—	IOA2 = √ 0, others: don't care	—	√	√
Output compare B function	√	—	—	√	—	—	—	—	—	IOB2 = √ 0, others: don't care	√	√
Input capture A function	√	—	—	PWM0 = 0	—	—	—	—	IOA2 = √ 1, others: don't care	—	√	√
Input capture B function	√	—	—	PWM0 = 0	—	—	—	—	—	IOB2 = √ 1, others: don't care	√	√
Counter Clear Function												
Clear at compare match/input capture A	√	—	—	√	—	—	—	—	√	√	CCLR1 = √ 0 CCLR0 = 1	√
Clear at compare match/input capture B	√	—	—	√	—	—	—	—	√	√	CCLR1 = √ 1 CCLR0 = 0	√
Synch-ronized clear	SYNCD = 1	—	—	√	—	—	—	—	√	√	CCLR1 = √ 1 CCLR0 = 1	√

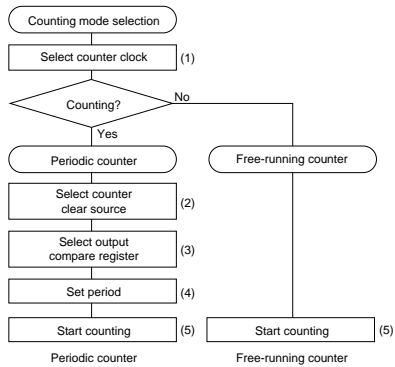
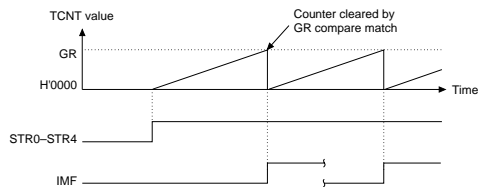
√: Settable, —: Setting does not affect current mode

1/21/99

Microcontroller Seminar -- ASH

23

Simple ITU Example

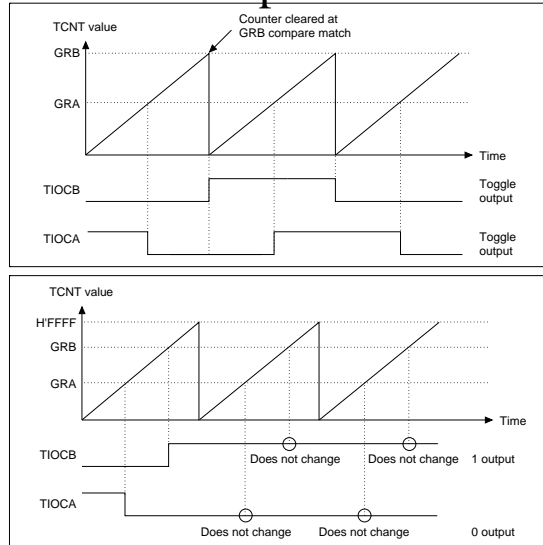


1/21/99

Microcontroller Seminar -- ASH

24

ITU output modes

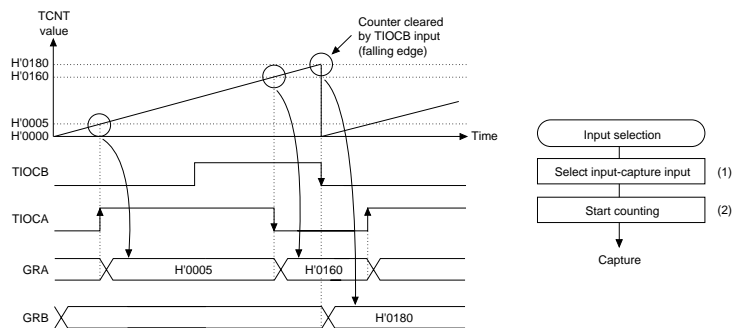


1/21/99

Microcontroller Seminar -- ASH

25

ITU measuring intervals

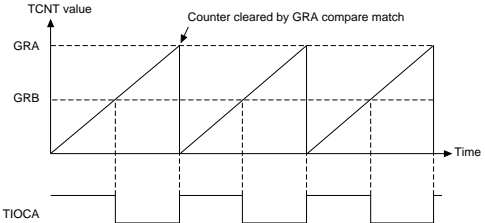
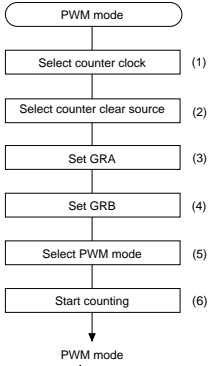


1/21/99

Microcontroller Seminar -- ASH

26

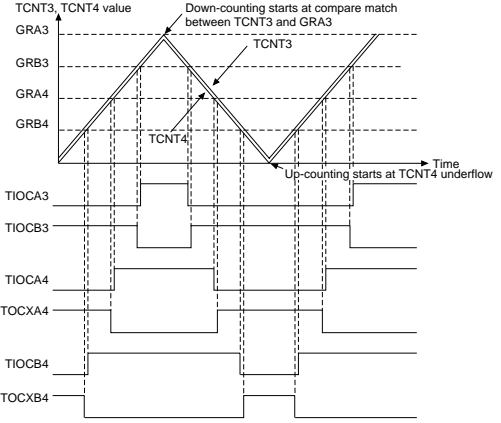
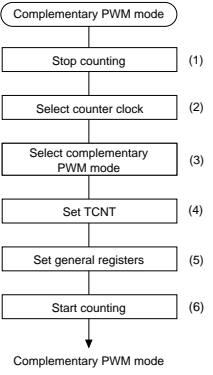
ITU in PWM mode



a. Counter cleared by GRA

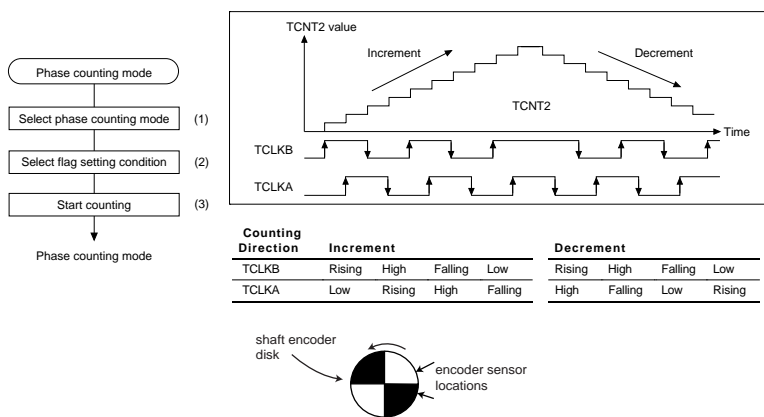
ITU complementary PWM mode

- Non-overlapping complementary PWM outputs



ITU in phase counting mode

- Use quadrature to figure out direction of rotation in shaft encoders



1/21/99

Microcontroller Seminar -- ASH

29

Direct Memory Access Controller

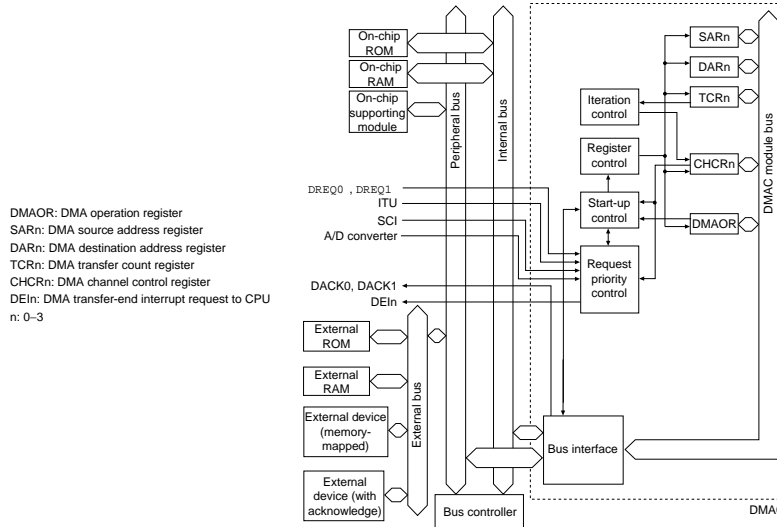
- 4-channel
 - 2 internal
 - 2 external
- 64K transfers at a time max.
- Addressing modes
 - single and dual address modes (for DREQ activated devices)
 - address increment of -2, -1, 0, 1, 2
- Transfer request modes
 - external from DREQ
 - internally generated signals from A/D, ITU, SCI
- Cycle steal and burst mode options
- Allows transfers to happen with no CPU loading

1/21/99

Microcontroller Seminar -- ASH

30

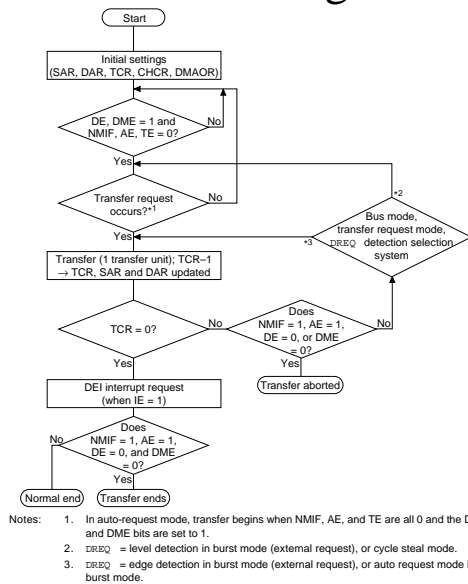
DMAC block diagram



DMAC registers

Chan- nel	Name	Abbrevi- ation	R/W	Initial Value	Address	Access Size
0	DMA source address register 0	SAR0 ³	R/W	Undefined	H5FFFF40	16, 32
	DMA destination address register 0	DAR0 ³	R/W	Undefined	H5FFFF44	16, 32
	DMA transfer count register 0	TCR0 ³	R/W	Undefined	H5FFFF4A	16, 32
	DMA channel control register 0	CHCR0	R/(W) ¹	H'0000	H5FFFF4E	8, 16, 32
1	DMA source address register 1	SAR1 ³	R/W	Undefined	H5FFFF50	16, 32
	DMA destination address register 1	DAR1 ³	R/W	Undefined	H5FFFF54	16, 32
	DMA transfer count register 1	TCR1 ³	R/W	Undefined	H5FFFF5A	16, 32
	DMA channel control register 1	CHCR1	R/(W) ¹	H'0000	H5FFFF5E	8, 16, 32
2	DMA source address register 2	SAR2 ³	R/W	Undefined	H5FFFF60	16, 32
	DMA destination address register 2	DAR2 ³	R/W	Undefined	H5FFFF64	16, 32
	DMA transfer count register 2	TCR2 ³	R/W	Undefined	H5FFFF6A	16, 32
	DMA channel control register 2	CHCR2	R/(W) ¹	H'0000	H5FFFF6E	8, 16, 32
3	DMA source address register 3	SAR3 ³	R/W	Undefined	H5FFFF70	16, 32
	DMA destination address register 3	DAR3 ³	R/W	Undefined	H5FFFF74	16, 32
	DMA transfer count register 3	TCR3 ³	R/W	Undefined	H5FFFF7A	16, 32
	DMA channel control register 3	CHCR3	R/(W) ¹	H'0000	H5FFFF7E	8, 16, 32
Shar-ed	DMA operation register	DMAOR	R/(W) ²	H'0000	H5FFFF48	8, 16, 32

DMAC Usage



1/21/99

Microcontroller Seminar -- ASH

33

Timing Pattern Controller

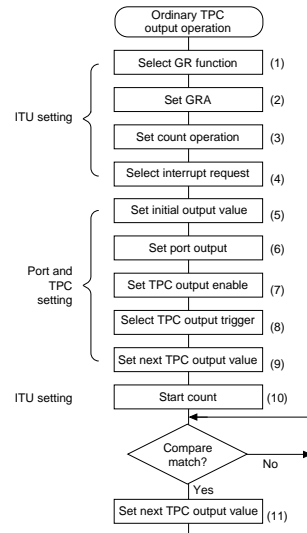
- 4 bits x 4 TPC units digital output
- typically used in conjunction with ITU and DMAC
- used to synthesize pulse trains whose details are determined by ITU timing and a sequence of bits stored in memory
 - good for doing serial protocols

1/21/99

Microcontroller Seminar -- ASH

34

TPC usage flow chart

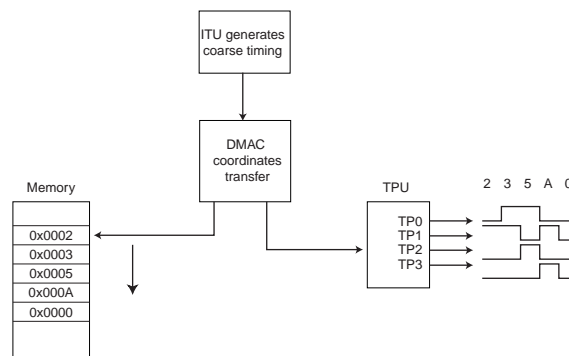


1/21/99

Microcontroller Seminar -- ASH

37

TPC + DMA + ITU example



1/21/99

Microcontroller Seminar -- ASH

38

A/D Converter

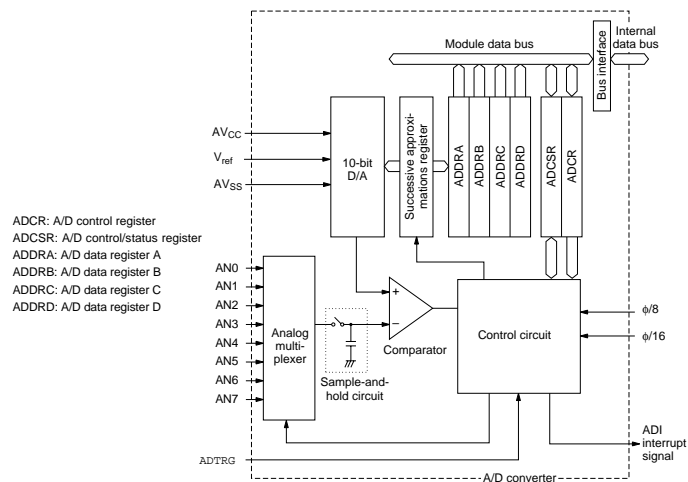
- 8 channels, multiplexed
- 10 bits/channel
- Integrated S/H with internal or external sample trigger
- Successive Approximation
- Vref tied to 2.5V on SH1WH => 2.44 mV/LSB
- 11.2 us per channel conversion rate
- Can trigger DMAC for background sampling
- Scan mode capable (sample from each channel round-robin style)
- polled or interrupt mode for A/D completion

1/21/99

Microcontroller Seminar -- ASH

39

A/D Converter Block Diagram



1/21/99

Microcontroller Seminar -- ASH

40

A/D converter registers

Register Name	Abbreviation	R/W	Initial Value	Address* 1	Access Size
A/D data register A (high)	ADDRAH	R	H'00	H'05FFFFE0	8, 16
A/D data register A (low)	ADDRAL	R	H'00	H'05FFFFE1	16
A/D data register B (high)	ADDRBH	R	H'00	H'05FFFFE2	8, 16
A/D data register B (low)	ADDRBL	R	H'00	H'05FFFFE3	16
A/D data register C (high)	ADDRCH	R	H'00	H'05FFFFE4	8, 16
A/D data register C (low)	ADDRCL	R	H'00	H'05FFFFE5	16
A/D data register D (high)	ADDRDH	R	H'00	H'05FFFFE6	8, 16
A/D data register D (low)	ADDRDL	R	H'00	H'05FFFFE7	16
A/D control/status register	ADCSR	R/(W)*2	H'00	H'05FFFFE8	8, 16
A/D control register	ADCR	R/W	H'7F	H'05FFFFE9	8, 16

1/21/99

Microcontroller Seminar -- ASH

41

Embedded RAM

- 8K of fast RAM
 - 1 cycle access time read/write
 - 32-bit wide datapath
- Use for inner loops and time-critical processing
 - like a user managed cache
- Located from 0xF000000 to 0xF002000

1/21/99

Microcontroller Seminar -- ASH

42

Power Down Modes

- Power down modes entered by executing SLEEP instruction
 - sleep or standby set by changing a bit in the SBYCR
- sleep mode
 - clock runs, CPU halts, all peripherals run
 - exit through interrupt, DMA address error, power on reset, manual reset
- standby mode
 - clock halts, all functions stop
 - exit through NMI, power on reset, or manual reset

1/21/99

Microcontroller Seminar -- ASH

43

Building a system

- Minimal SH-1 system
 - SH-1 + embedded ROM/RAM, crystal
- SH1WH system
 - SH-1
 - 8 MB DRAM
 - 128K battery backed SRAM
 - 1 MB ISP FLASH
 - D/A converter
 - RTC
 - RS-232 transceivers
 - Extra digital I/O
 - Switching regulator

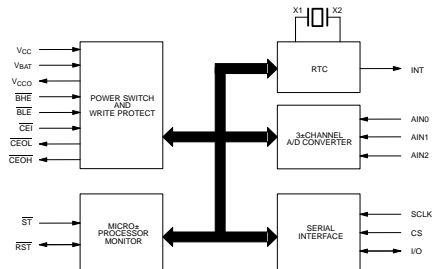
1/21/99

Microcontroller Seminar -- ASH

44

SH1WH RTC

- Dallas Semiconductor DS1670 system controller/RTC
- Serial interface to RTC
 - CLK, DIN/DOUT, CS
- Power fail manager
 - turns of SRAM CS, resets processor on low Vcc condition
- 3-channel, 8-bit A/D converter
 - used for temperature sensor
- Wake-up alarm clock
- Watchdog timer



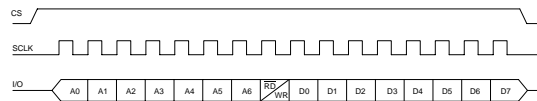
1/21/99

Microcontroller Seminar -- ASH

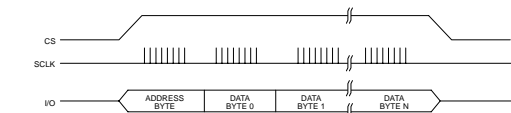
45

RTC registers, serial interface

SINGLE BYTE DATA TRANSFER



MULTIPLE BYTE BURST TRANSFER



BIT7										BIT0
00	0	10 SECONDS				SECONDS				
01	0	10 MINUTES				MINUTES				
02	0	12	24	10 HR	10 HR	HOURS				
03	0	0	0	0	0	DAY				
04	0	0	10 DATE			DATE				
05	0	0	0	10 MO.			MONTH			
06	10 YEAR				YEAR					
07	M	10 SEC ALARM				SECONDS ALARM				
08	M	10 MIN ALARM				MINUTES ALARM				
09	M	12	24	10 HR	10 HR	HOUR ALARM				
0A	M	0	0	0	0	DAY ALARM				
0B	CONTROL REGISTER									
0C	STATUS REGISTER									
0D	WATCHDOG REGISTER									
0E	ADC REGISTER									
0F	RESERVED									
7F										

1/21/99

Microcontroller Seminar -- ASH

46

D/A converter

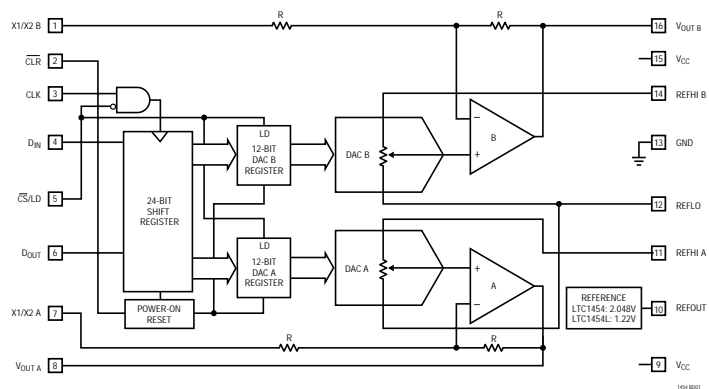
- LTC1454L D/A converter
 - 12-bit resolution
 - 1.220V reference + x2 amplifier => 2.44V effective full-scale
 - power-on reset to 0
 - 14 us typ. settling time, 1 V/us typ. slew rate

1/21/99

Microcontroller Seminar -- ASH

47

D/A converter

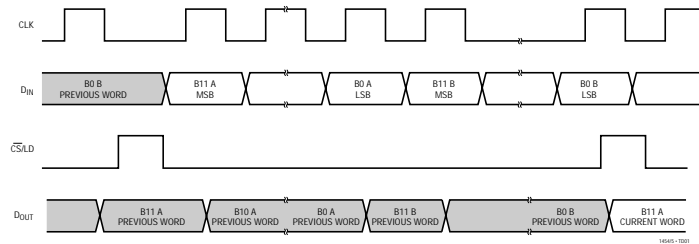


1/21/99

Microcontroller Seminar -- ASH

48

D/A converter



1/21/99

Microcontroller Seminar -- ASH

49

FLASH ROM

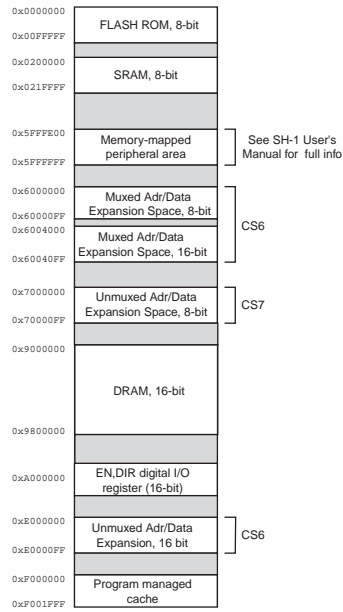
- 1 MB, 3.3V only boot-block ROM with autoshtutdown
- embedded algorithms for erase and program
 - writing a special sequence to the FLASH causes erasing and programming to occur
- like all FLASH, an entire sector must be erased before being written to
 - erase defaults to '1'
 - programming will clear respective bits to '0'
 - possible to program over if all you're doing is setting bits to 0
- drivers provided for your convenience in using the FLASH
 - not recommended to muck around too much with the boot block, as losing the boot block means you'll have to desolder the ROM and burn it in a programmer

1/21/99

Microcontroller Seminar -- ASH

50

SH1WH Memory Map

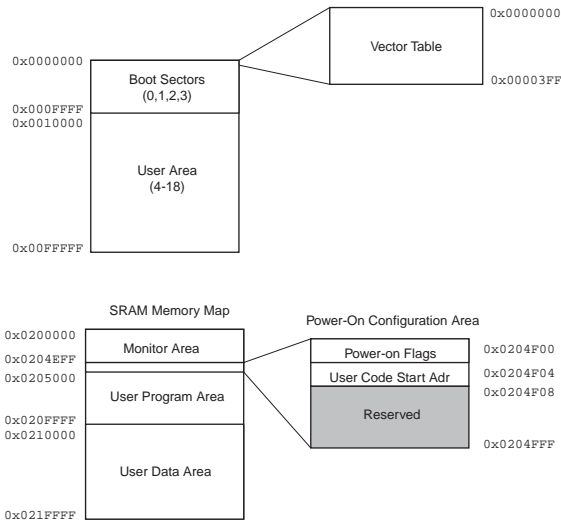


1/21/99

Microcontroller Seminar -- ASH

51

SRAM and FLASH Memory Map



1/21/99

Microcontroller Seminar -- ASH

52

Development Environment

- Host environment
 - GNU development environment
 - gcc, make, binutils, etc.
 - cross-compiler to SH-COFF format can be built for a large number of platforms
 - all software developed under Linux 2.0.32 with emacs as editor
 - DOS version of development environment to be released soon
 - java applet called JTerm which runs under windows is used to upload code binaries and interact with monitor
 - any serial terminal program can do interaction, but upload protocol is proprietary (basically straight binary plus header and trailer bytes)
 - uses Sun javax.comm extensions, only supports windows and Sun OS platforms but will be part of java spec soon
 - communication via serial port, 38400 N81

1/21/99

Microcontroller Seminar -- ASH

53

Development Environment

- Target environment
 - Interactive ROM monitor available at all times
 - manipulate and examine memory, registers, code
 - base level diagnostics
 - User settable power-on environment
 - can go straight to user code in battery-backed SRAM or FLASH for stand-alone operation
 - can go straight into monitor for debugging operations
 - panic mode to drop into monitor in case user code fails
 - FLASH burning, RTC manipulation, FPGA programming all provided as uploadable binaries
 - Code development starts with a set of template files which contains necessary code to initialize SP, jump to main; you just need to add your code and compile

1/21/99

Microcontroller Seminar -- ASH

54

Development Environment

- Things to avoid doing:
 - Don't bash the FLASH, particularly the ROM monitor area
 - Don't set the RTC watchdog timer unless you have code to turn it off
 - Doing either of the above will require desoldering components or pins off of the board to recover from